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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Sheet 1

of 2

Complete if Known

Application Number	09/997,530
Filing Date	11/30/2001
First Named Inventor	MASTER, Paul L. et al.
Art Unit	2183
Examiner Name	Pan, Daniel H.
Attorney Docket Number	QuickSilver Technology

U. S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
/D.P./		US- 5,450,557	09/12/1995	Kopp et al.	Col. 1 - 4
		US- 6,047,115	04/04/2000	Mohan et al.	Col. 3 - 5
		US- 5,479,055	12/26/1995	Eccles	Col. 1 - 3
		US- 6,433,578	08/13/2002	Wesson	Col. 6-8
		US- 5,963,048	10/05/1999	Harrison et al.	Fig. 4
		US- 4,694,416	09/15/1987	Wheeler et al.	Col. 2- 6
		US- 6,282,627	08/28/2001	Wong et al.	Col. 2, 4, 5
		US- 6,353,841	03/05/2002	Marshall et al.	Col. 6, Fig. 3
		US- 5,910,733	06/08/1999	Bertolet et al.	Col. 5, 7
		US- 5,886,537	03/23/1999	Macias et al.	general background
		US- 6,538,470	03/25/2003	Langhammer et al.	Col. 2- 6
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		US- 5,956,518	09/21/1999	DeHon et al.	Fig. 6
		US- 6,556,044	04/29/2003	Langhammer et al.	Col. 2- 4
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FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ³
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Examiner Signature	/Daniel Pan/	Date Considered	02/19/2008
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				Attorney Docket Number	QuickSilver Technology

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
/D.P./		ZHANG, HUI et al., "A 1V Heterogeneous Reconfigurable Processor IC for Baseband Wireless Applications", 2000 IEEE Solid-State Circuits Conference, 7 February 2000, pp. 68-69, XP010378803, ISBN: 07803-5853-8/00	
		ALSOLAIM, A et al., "Architecture and Application of a Dynamically Reconfigurable Hardware Array for Future Mobile Communication Systems", Field Programmable Custom Computing Machines, 2000 IEEE Symposium, Napa Valley, Los Alamitos, CA 17-19 April 2000, IEEE Comput. Soc., 17 April 2000, pp. 205-214, XP010531939, ISBN 0-7695-0871-5/00	
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		ABNOUS A. et al., "Ultra-low-power domain-specific multimedia processors", VLSI SIGNAL PROCESSING, IX, 1996, IEEE WORKSHOP IN SAN FRANCISCO, CA, USA, 30 Oct - 1 Nov. 1996, 30 October 1996, pp. 461-470, XP010199037, ISBN: 0-7803-3134-6.	
		BAUMGARTE, V. et al., "PACT XPP - A Self-Reconfigurable Data Processing Architecture", NN, 25 June 2001, XP002256066	
		HARTENSTEIN, R. "Coarse Grain Reconfigurable Architectures", Design Automation Conference, 2001. Proceedings of the ASP-DAC 2001, Asia and South Pacific 30 Jan-2 Feb 2001, Piscataway, NJ, US, IEEE 30 Jan 2001, pp. 564-569, XP010537867, ISBN: 0-7803-6833-6	

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